ABSTRACT

A memory system architecture/interconnect topology includes a configurable width buffered module having a configurable width buffer device. The configurable width buffer device is coupled to at least one memory device on the configurable width memory module. The configurable width buffer device includes an interface and a configurable serialization circuit capable of varying a data path width or a number of contacts used at the interface of the configurable width buffer device in accessing the at least one memory device. In an alternate embodiment of the present invention, a multiplexer/demultiplexer circuit is provided. A state storage provides a data width for the configurable width buffer and a SPD provides the configurable width buffer and/or module capabilities to the memory system.